MARKED-UP VERSION OF THE AMENDED CLAIMS

A marked-up version of the amended claims 31, 33, and 35 is provided below. Additions are indicated with "__" and deletions are indicated within "[ ]."

31. (Three Times Amended) A memory device, comprising:

a memory array;

a register to store at least one bit indicating a suspend status of a write operation for the memory array; and

a control circuit coupled to said memory array and said register, said control circuit to update said register and to control [the] an output of a status signal representing said [protection] suspend status of [a data modification] said write operation, and wherein said control circuit includes:

a first state machine to receive commands for accessing said memory array or said register, and

a second state machine coupled to said first state machine and to execute the commands received by said first state machine.

32. (Unchanged) The memory device of claim 31, wherein said write operation represents a byte write operation.

33. (Amended) The memory device of claim 31, wherein said [suspend] status signal represents a byte write suspend command.

34. (Unchanged) The memory device of claim 31, wherein said control circuit is to receive a status request signal and said register is to output said status signal in response to said status request signal, said status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

35. (Amended) The memory device of claim 31 [35], further comprising:

at least one data input/output coupled to said control circuit, wherein the at least one data input/output is to receive said status request signal from a processor and to provide said status signal to said processor.

36. (Unchanged) The memory device of claim 31, further comprising:

a status output coupled to said register, wherein said status output is to provide a second status signal if said status output is polled, and wherein said second status signal having a first state to indicate said write operation is suspended and a second state to indicate said write operation is not suspended.

37. (Unchanged) The memory device of claim 31, wherein said status request signal is a read status register command.

REMARKS

Reconsideration of this application, as amended, is respectfully requested. The following remarks are responsive to the Office Action mailed February 27, 2001.

Claims 31-37 are pending.

Claims 31, 33, and 35 have been amended to correct for antecedent and claim dependency problems. Applicants respectfully submit that the amendments made herein do not add new matter.

Claims 31-37 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over applicants' admitted prior art or to U.S. Patent No. 5,561,628 to Terada *et al.* ("Terada").

Claims 31-37 stand rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 5,937,424 to Leak *et al.* ("Leak") in view of Terada.

35 U.S.C. § 103(a) Rejection - Admitted Prior Art and Terada

The Examiner has rejected claims 31-37 as being unpatentable over applicants' admitted prior art or to Terada. In particular, the Examiner states:

> Applicant's admitted prior art teaches that it was known in the prior art to suspend flash memory erase cycles because of the length of time required for the erase cycle (see specification, lines 1-2). Further, applicants admit that status registers typically store data indicative of the current device status, including whether or not an erase operation has been suspended (see figure 1, memory location 104, "ESS"). Applicants also admit that the stored status was output when the device was polled or in response to a read status register command (see specification, page 2, lines 3-7). The memory array in applicant's described prior art is understood. Applicants do not admit that suspension of a programming operation was taught in the prior art. However, while a programming operation does not take as long as an erase operation, it still takes a significant amount of time relative to data read operation (7-8 microseconds as opposed to 85 nanoseconds, see specification, page 1, lines 22-25). It would have been obvious at the time the invention was made to a person having ordinary

skill in the art to which said subject matter pertains to have modified applicant's admitted prior art to include the ability to suspend programming operations to improve the overall performance of a flash memory device. Such a modification, would clearly involve the modification of the status register to include at lease one bit to indicate the suspension status of a programming operation (e.g., a "PSS" bit similar to the admitted "ESS" bit). Applicants do not discuss the existence in the prior art of a control circuit including a first state machine for receiving commands to access the memory array or the status register and a second state machines to execute the command received by the first state machine. However, such implementation is typical, i.e., a command decoder (i.e., a first state machine) is required to determine what type of command has been received, whether it is a valid command, whether it can be executed, etc. If the command can indeed be executed, the command is typically sent to circuitry specific to the execution of the command (i.e., a second state machine). Clearly applicant's admitted prior art receives a command (i.e., "when polled" or "in response to a read status register command", see specification, page 2, lines 4-7) and then executes the command (i.e., "the status signal may be sent...via a designated output pin" or "via the data input/output ('I/O') pins", *ibid*). It is inherent that applicant's admitted prior art includes the claimed first and second state machines. Further, the admitted prior art programming operation inherently would have included a "byte write" (or "byte program") instruction (claim 32) since that was the typical manner of writing to flash memories. Obviously that would be the programming operation to suspend (claim 33). It is also obvious that the status register read operation of applicant's admitted prior art would output the contents of the status register as modified above, including the write suspend status (claim 34). A device as described above would inherently include the ability to input requests and output data (claim 35). Applicant's admitted prior art includes the ability to be polled or receive a read status register command, it would have been obvious to retain such abilities (claims 36 and 37).

The Terada *et al.* references teaches, *inter alia*, flash EEPROMs (see figure 3, flash memories 40a through 40d) with the ability to suspend erase cycles, and a status register that outputs an erase suspend status signal when the status register is read (see column 10, lines 47-59 and tables 1 and 2. The memory array *per se* is understood. Terada does not teach the suspension of a programming operation. However, while a programming operation does not take as long as an erase operation, it still takes a significant amount of time relative to data read operation. In a particular 8M-bit IC card it "takes one second or less to read all the addresses on one flash memory, 9.6 seconds to write in all the addresses in one flash memory, and 25.6 seconds to erase from all the addresses of one flash memory", see column 5, lines 5-11). It would have been obvious at

the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modified the memories taught by Terada to include the ability to suspend programming operations to improve the overall performance of a flash memory device. Such a modification, would clearly involve the modification of the status register to include at least one bit to indicate the suspension status of a programming operation (e.g., a "PSS" bit similar to bit 6, "ESS", see tables 1 and 2). Terada does not discuss a control circuit including a first state machine for receiving commands to access the memory array or the status register and a second state machines to execute the command received by the first state machine. However, such implementation is typical, i.e., a command decoder (i.e., a first state machine) is required to determine what type of command has been received, whether it is a valid command, whether it can be executed, etc. If the command can indeed be executed, the command is typically sent to circuitry specific to the execution of the command (i.e., a second state machine). Clearly Terada's flash memories receive a command (i.e., "can be read", see column 10, lines 53-55) and then executes the command (i.e., "via a data bus for transmitting signals D0 to D15", *ibid*). It is inherent that Terada includes the claimed first and second state machines. Further, each of the Terada flash memories operates in a "byte write" (or "byte program") mode (see table 2, SR.4, claim 32). Obviously that would be the programming operation to suspend (claim 33). It is also obvious that Terada's status register read operation would output the contents of the status register as modified above, including the write suspend status (claim 34). A device as described above would inherently include the ability to input requests and output data (claim 35). Terada's flash memories clearly can be polled or otherwise (claims 36 and 37).

(p. 2-5 Office Action 2/27/01).

Applicants respectfully submit the claim 31, as amended, is not obvious over applicants' admitted prior or to Terada. For claim 31 to be rendered obvious, applicants' admitted prior art or Terada must disclose or suggest each and every limitation of the claim. Claim 31 includes the following limitations:

> 31. A memory device, comprising:
> a memory array;
> a register to store at least one bit indicating a suspend status of a write operation for the memory array; and
> a control circuit coupled to said memory array and said register, said control circuit to update said register and to control an output of a

status signal representing said suspend status of said write operation, and wherein said control circuit includes:

a first state machine to receive commands for accessing said memory array or said register, and

a second state machine coupled to said first state machine and to execute the commands received by said first state machine.

(Claim 31)(emphasis added).

A distinction of claim 31 over applicants' admitted prior art and Terada is a register to store at least one bit indicating a suspend status of a write operation for the memory array as recited in claim 31.

Figure 1 of applicants' disclosure shows a prior art status register 100 having a memory location 104 for an erase suspend status ("ESS") information. The prior art status register 100, however, does not disclose or suggest a register to store at least one bit indicating a suspend status of a write operation as recited in claim 31.

Furthermore, applicants respectfully submit that the Examiner has incorrectly directed obviousness to claim 31 with respect to applicants' admitted prior art. In particular, the Examiner indicates that it would have been obviousness to incorporate the ability to suspend "programming operations" with applicants' admitted prior art. (See p.3 Office Action 2/27/01). Claim 31, however, recites at least one bit of a register indicating a suspend status of a write operation.

Terada, in Figure 1, discloses an IC card having flash memories 40a and 40d with a status register 41. Status register 41 includes 8 bits in which bit 6 indicates a status for an "erase suspend" status. Claim 31, however, recites a register to store at least one bit indicating a suspend status of a write operation.

Furthermore, applicants respectfully submit that the Examiner has incorrectly directed obviousness to claim 31 with respect to Terada. In particular, the Examiner indicates that it would have been obviousness to incorporate the ability to suspend "programming operations" with Terada. (See p.4 Office Action 2/27/01). Claim 31, however, recites at least one bit of a register indicating a suspend status of a write operation.

Therefore, neither applicants' admitted prior art nor Terada individually or in combination disclose or suggest the above distinction of claim 31.

Another distinction of claim 31 over applicants' admitted prior art and Terada is a control circuit coupled to said memory array and said register, and said control circuit to update said register and to control an output of a status signal representing said suspend status of said write operation.

Figure 1 of applicants' disclosure does not show a control circuit as recited in claim 31. Instead, Figure 1 shows a prior art status register 101 with five status locations, and one of the locations is for an "erase suspend" status. Terada, however, does not disclose a control circuit that outputs a status signal representing a suspend status of a write operation as recited in claim 31. Terada, like the admitted prior art, discloses a suspend status for an erase operation and not a write operation as recited in claim 31.

Therefore, neither applicants' admitted prior art nor Terada individually or in combination disclose or suggest the above distinction of claim 31.

Still another distinction of claim 31 over applicants' admitted prior art and Terada is a control circuit including a first state machine to receive commands for accessing said

memory array or said register, and a second state machine coupled to said first state machine and to execute the commands received by said first state machine.

Applicants' admitted prior art (i.e., Figure 1) and Terada are clearly deficient in showing or suggesting the first and second state machines as recited in claim 31. The Examiner states that the claimed first and second state machines are inherent in the applicants' admitted prior art and Terada. Applicants' respectfully disagrees for the following reasons.

First, inherency may not be relied upon to incorporate "missing" structure. In particular, inherency can be used to teach a missing characteristic of a thing described in a reference.[1] This is not the case. Here, the Examiner admits that neither applicants' admitted prior art nor Terada disclose the first and second state machines as recited in claim 31. Because the claimed first and second state machines are not disclosed in applicants' admitted prior art and Terada, the Examiner relies on inherency to teach such elements, which is improper.

Second, even if inherency could be used to teach using state machines, applicants' admitted prior art and Terada still do not teach or suggest a control circuit to an output of a status signal representing said suspend status of said write operation as recited in claim 31.

Therefore, neither applicants' admitted prior art nor Terada individually or in combination disclose or suggest the above distinction of claim 31. For all of the above distinctions, claim 31 is patentable over applicants' admitted prior art and Terada and is

[1] See. M.P.E.P. § 2112 (citing, e.g., *In re Ricjckaert*, 9 F.3d 1531 (Fed. Cir. 1993); *In re Oelrich*, 666 F.2d 578 (CCPA 1981); *In re Robertson*, 169 F.3d 743 (Fed. Cir. 1999); *Ex parte Levy*, 17 USPQ2d 1461 (Bd. Pat. App. & Inter. 1990); *In re Schreiber*, 128 F.3d 1473 (Fed. Cir. 1997)).

in condition of allowance. Given that claims 32-37 depend on claim 31, applicants respectfully submit that claims 32-37 are patentable over applicants' admitted prior art and Terada and are in condition of allowance.

35 U.S.C. § 103(a) Rejection - Leak in view of Terada

The Examiner has rejected claims 31-37 as being unpatentable over Leak in view of Terada. In particular, the Examiner states:

> The Leak *et al.* reference teaches a memory device which includes a memory array (understood), a register to store status information (see figure 7B, status register 142), a control circuit including a command decoder (first state machine) and a second state machine see figure 7B, any of elements 190, 192, 194, 195, 196 and 198. The reference further teaches that it is advantageous to be able to suspend both erase and write operations. The reference does not teach the particulars of the status register. The Terada reference has been discussed above. It teaches a status register that includes an "ESS" bit to indicate the erase suspend operation status. It would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains to have modeled Leak the status register after the Terada status register to include an "ESS" bit to indicate that an erase operation has been suspended, and to further have modified the Terada status register to include a "WSS" bit to indicate that a write operation has been suspended. By the comparisons to the prior art, it appears that Leak operates in byte write mode and that the byte write operation is suspended (claims 32 and 33). In keeping with the modification above, note that Terada teaches that if ESS = 1, an erase operation is suspended, if EEE = 0, then no erase is suspended. The above modification would, by analogy, indicate that if WWW = 1, then a write operation is suspended and if WSS = 0, then no write operation is suspended (claim 32). The Leak command decoder has an input and clearly receives a status request signal to activate read status circuitry 198 (see figures 7A and 7B). The status register apparently outputs the status data on line RY/BY# (see figure 7B), presumably only upon request (claims 36 and 37).

(p. 6-7 Office Action 2/27/01)

Applicants respectfully submit the claim 31, as amended, is not obvious over Leak in view of Terada. For claim 31 to be rendered obvious, Leak and Terada must

individually or in combination teach each and every limitation of claim 31. Furthermore, there must be some motivation or suggestion to combine Leak with Terada.

Applicants respectfully submit that the above distinctions of claim 31 noted above are also distinctions over Leak in view of Terada.

In particular, Leak discloses in FIG. 6 a status register 142. Leak, however, does not teach or suggest a register having a bit indicating a suspend status of a write operation as recited in claim 31, which the Examiner admits. Furthermore, Leak discloses a command decoder 170 to clear command latches 176a-n. Leak does not disclose a control circuit to update a register and to control an output of a status signal representing said suspend status of said write operation as recited in claim 31. In addition, Lead does not disclose the claimed first and second state machines as recited in claim 31.

Terada fails to cure the deficiencies of Leak. As noted previously, Terada discloses a status register 41 having 8 bits in which bit 6 indicates a status for an "erase suspend." Terada, however, does not teach or suggest status register 41 having a bit for "suspend status" of a "write operation". Terada also does not disclose or suggest the claimed control circuit including a first and second state machines as recited in claim 31.

It is also respectfully submitted that Leak does not disclose or suggest a combination with Terada. Furthermore, Terada does not disclose or suggest a combination with Leak. Applicants' respectfully submit that that it would be impermissible hindsight based on applicants' own disclosure to incorporate Leak with Terada. Moreover, even if Leak and Terada are combinable, such a combination would

still fail to disclose or suggest the status register and control circuit as recited in claim 31.

Therefore, for the above reasons, claim 31 is patentable over Leak in view of Terada and is in condition of allowance. Given that claims 32-37 depend on claim 31, applicants respectfully submit that claims 32-37 are patentable over Leak in view of Terada and are in condition of allowance.

It is respectfully submitted that in view of the amendments and remarks set forth herein, the above 35 U.S.C. § 103(a) rejections have been overcome. Accordingly, applicants respectfully request that claims 31-37 be found in a condition of allowance.

If a telephone interview would expedite the prosecution of this application, the Examiner is invited to contact Mike Kim at (408) 947-8200 x212.

If there are any additional charges, please charge them to our Deposit Account No. 02-2666.

Respectfully submitted,

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